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10/727,645	12/05/2003	Yoshinori Ogawa	12480-000030/US	8967

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SITTA, GRANT	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/727,645	OGAWA ET AL.	
	Examiner	Art Unit	
	Grant D. Sitta	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :11/28/2005,8/22/2005,12/05/2003.

DETAILED ACTION

Drawings

1. Figures 7,8a,8b,9,20,21,22, and 23 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 15 rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Subject matter which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976)..

4. In claim 15, lines 3-5 the recitation of the claim "an input operation circuit [0033-0034].However, this term is not widely accepted in the art and its discloser in the

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 4, 6 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. In regards to claim 4, it is unclear what "supplying circuit supplies the common electrode voltage of an equal value to each other" page 96, last paragraph.

5. In regards to claim 6, it is unclear what "grouped for n lines of the scanning lines (n includes one), where n is a positive integer." page 97, claim 6.

6. In regards to claim 34, it is unclear what "sequentially grouped for n lines of the scanning lines (n includes one), where e is a positive integer." Page 110, claim 34.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1,2 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakao (2001/0003431) hereinafter, Nakao.

3. In regards to claim 1, Nakao teaches a liquid crystal display device (fig. 6 (1)), comprising: a plurality of scanning lines (fig. 7 (15)); a plurality of signal lines (fig. 7 (14)) provided so as to cross the scanning signals (fig. 7 intersection of 14 and 15); a liquid crystal layer having liquid crystal molecules, aligned in random directions throughout a liquid crystal panel, each of which has a substantially fixed twist angle in a direction perpendicular to substrates sandwiching the liquid crystal layer (fig. 7 inherent); pixel capacitors (fig. 7 (12)), respectively formed on pixels corresponding to intersections of the scanning lines and the signal lines (fig. 7 14 and 15), which include pixel electrodes and common electrodes ([004] "an opposite electrode (common electrode)"), and correspond to the liquid crystal layer [0007]; and a common electrode voltage [0007] supplying circuit for supplying common electrode voltages to the common electrodes ([0007] "The LCD panel 1 has pixel electrodes 11, pixel capacitors 12, TFTs 13 for controlling the turning-on and -off of a voltage to be applied to the pixel electrodes 11, source signal lines 14, gate signal lines 15") said common electrode Voltage supplying circuit being capable of adjusting (abstract, "A gamma correction adjustment circuit 42 adjusts the gamma-corrected intermediate voltages upward or downward")the common electrode voltages ([0007] on and off of voltage).

4. In regards to claim 28, a plurality of scanning lines (fig. 6 lines from (4)) ; a plurality of signal lines (fig. 6 lines from (3)) provided so as to cross the scanning signals (fig. 7 (1)); pixel capacitors (fig. 7 (12)), having pixel electrodes and common electrodes

(fig. 7 (11)), and corresponding to a liquid crystal layer (fig. 6 (LCD)), which are respectively formed on pixels corresponding to intersections of the scanning lines and the signal lines (fig. 7 (14 and 15)), wherein the liquid crystal layer has liquid crystal molecules (fig. 6 (LCD)), aligned in random directions throughout a liquid crystal panel (inherent with Liquid crystal material), each of which has a substantially fixed twist angle in a direction perpendicular to substrates for sandwiching the liquid crystal layer (fig. 6 (LCD)), said method comprising the step of supplying common electrode voltages and adjusting the common electrode voltages. (abstract "Resistor elements R0 through R7 have a resistance ratio for gamma correction and generate gamma-corrected intermediate voltages on the basis of voltages across both input terminals V0 and V64. A gamma correction adjustment circuit 42 adjusts the gamma-corrected intermediate voltages upward or downward on the basis of adjustment data latched in a data latch circuit 43. By thus supplying the adjustment data corresponding to the liquid crystal material and the LCD panel characteristics to the data latch circuit 43, the gamma correction characteristic can be changed in accordance with the liquid crystal material")

5. In regard to claim 2, Nakao teaches the common electrodes of the pixels are divided into a plurality of groups, and the common electrode voltage supplying circuit is capable of respectively adjusting the common electrode voltages so that the common electrode voltages are adjusted independently every groups ((fig. 11 V64-V0) and [0015 This gray scale display reference voltage generating circuit 39 is constructed of nine

gray scale voltage input terminals indicated by V0, V8, V16, V24, V32, V40, V48, V56 and V64, resistor elements R0 through R7 having a resistance ratio for gamma correction and a total of 64 resistors (not shown) that are in groups of eight serially connected across both terminals of the resistor elements R0 through R7. As described above, the resistance ratio called the gamma correction is built into the source driver, providing the LCD drive output voltage for conversion into the gray scale display voltage with a line graph characteristic.")

6. Claims 3-27 and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakao, in view of Hisao (JP 05-053534) hereinafter, Hisao.

7. In regards to claim 3, Nakao discloses the limitations of claim 1 and and the common electrode voltage supplying circuit is capable of respectively independently adjusting a common electrode voltage supplied to common electrodes corresponding to the first pixel capacitors and common electrode voltages supplied to common electrodes corresponding to the second pixel capacitors (fig. 1 V64 and adjustment data),

Nakao differs from the claimed invention in that Nakao does not disclose at least first pixel capacitors and second pixel capacitors are provided on each of the pixels as the pixel capacitors

However, Hisao teaches a system and method for at least first pixel capacitors and second pixel capacitors are provided on each of the pixels as the pixel capacitors ((fig. 12 Cgd, Clc or Cs).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Nakao to include the use of capacitors as taught by Hisao in order to hold a charge.

8. In regards to claim 4, Hisao teaches the common electrodes [0005] corresponding to the second pixel capacitors are divided into a plurality of groups, and the common electrode voltage supplying circuit supplies the common electrode voltage of an equal value to each other to the common electrodes corresponding to the first pixel capacitors, and is capable of respectively adjusting the common electrode voltages supplied to the common electrodes corresponding to the second pixel capacitors independently every groups ([0008] fig. 13).

9. In regard to claim 5, Hisao teaches the common electrodes corresponding to the first pixel capacitors are divided into a plurality of groups, and the common electrode corresponding to the second pixel capacitors are divided into a plurality of groups, and the common electrode voltage supplying circuit (fig. 8 Vcom) is capable of respectively adjusting the common electrode voltage supplied to the common electrodes corresponding to the first pixel capacitor (fig. 12 (Vlc)) independently every groups and

is capable of respectively adjusting the common electrode voltages supplied to the common electrodes corresponding to the second pixel capacitors independently ever groups [0008].

10. In regards to claim 6, Nakao teaches wherein the common electrodes are grouped for n lines of the scanning lines (n includes one), where n is a positive integer (fig. 1 lines for (41).

11. In regards to claim 7, Nakao teaches wherein the common electrodes are grouped for n lines of the scanning lines (n includes one), where n is a positive integer (fig. 1 lines for (41).

12. In regards to claim 8, Nakao teaches the common electrode voltage supplying circuit supplies a common electrode voltage which functions as a reference common electrode voltage to a group corresponding to a scanning line positioned on the one side in a direction in which the scanning signals are disposed, and the common electrode voltage supplying circuit supplies a common electrode voltage which has a value different from a value of the reference common electrode voltage to a group corresponding to a scanning line positioned on the other side in the direction in which the scanning signals are disposed (fig. 2 (42) and [0069]).

13. In regards to claim 9, Nakao teaches wherein: the common electrode voltage supplying circuit supplies a common electrode voltage which functions as a reference common electrode voltage to a group corresponding to a scanning line positioned on the one side in a direction in which the scanning signals are disposed, and the common electrode voltage supplying circuit supplies a common electrode voltage which has a value different from a value of the reference common electrode voltage to a group corresponding to a scanning line positioned on the other side in the direction in which the scanning signals are disposed (fig. 2 (42) and [0069]).

14. In regards to claim 10, Nakao teaches wherein: the common electrode voltage supplying circuit supplies a common electrode voltage which functions as a reference common electrode voltage to a first group corresponding to a scanning line centered in a direction in which the scanning lines are disposed, and the common electrode voltage supplying circuit supplies a common electrode voltages which is higher than the reference common electrode voltage to a second group corresponding to a scanning line positioned on the one side in the direction in which the scanning lines are disposed, (fig. 2 (42) and [0069]) and the common electrode voltage supplying circuit supplies a common electrode voltage which is lower [0071] than the reference common electrode voltage to a third group corresponding to a scanning line positioned on the other side in the direction in which the scanning lines are disposed [0071-0076].

15. In regards to claim 11, Nakao teaches the common electrode voltage supplying circuit supplies a common electrode voltage which functions as a reference common electrode voltage to a first group corresponding to a scanning line centered in a direction in which the scanning lines are disposed, and the common electrode voltage supplying circuit supplies a common electrode voltages which is higher than the reference common electrode voltage to a second group corresponding to a scanning line positioned on the one side in the direction in which the scanning lines are disposed (fig. 2 (42) and [0069]), and the common electrode voltage supplying circuit supplies a common electrode voltage which is lower [0071] than the reference common electrode voltage to a third group corresponding to a scanning line positioned on the other side in the direction in which the scanning lines are disposed [0071-0076].

16. In regards to claim 12, Hisao comprising a signal line driving circuit for supplying a display signal voltage to each of the signal lines, wherein the common electrode voltage supplying circuit is provided in the signal line driving circuit (fig. 6, (1)).

17. In regards to claim 13, Hisao teaches wherein the common electrode voltage supplying circuit adjusts the common electrode voltages supplied to the groups so that luminance of the pixels gradually varies so as to be monotonously darker or so as to be

monotonously brighter from one end side to a center of the scanning lines in a direction in which the scanning lines are disposed [0029-0031].

18. In regards to claim 14, Hisao teaches wherein the common electrode voltage supplying circuit adjusts the common electrode voltages supplied to the groups so that luminance of the pixels gradually varies so as to be monotonously darker or so as to be monotonously brighter from one end side to a center of the scanning lines in a direction in which the scanning lines are disposed [0029-0031].

19. In regards to claim 15, Nakao teaches wherein the common electrode voltage supplying circuit includes an input operation circuit which allows adjustment amounts of the common electrode voltages to be inputted (fig. 10 (31)).

20. In regards to claim 16, Hisao teaches wherein the common electrode voltage supplying circuit adjusts the common electrode voltages so that luminance and color variation of the pixels are corrected so that a visual angle with respect to a liquid crystal panel, viewed from an arbitrary position, is wider than a visual angle in a case where the common electrode voltages of all the groups are equal to each other [0006-0018].

21. In regards to claim 17, Hisao teaches wherein the common electrode voltage supplying circuit adjusts the common electrode voltages so that luminance and color variation of the pixels are corrected so that a visual angle with respect to a liquid crystal panel, seen from an arbitrary position in an up-and-down direction, is wider than a visual angle in a case where the common electrode voltages of all the groups are equal to each other [0006-0018].

22. In regards to claim 18, Hisao teaches wherein the common electrode voltage supplying circuit adjusts the common electrode voltages so that luminance and color variation of the pixels are corrected so that a visual angle with respect to a liquid crystal panel, seen from an arbitrary position, is wider than a visual angle in a case where the common electrode voltages of all the groups are equal to each other [0006-0018].

23. In regards to claim 19, Hisao teaches wherein the common electrode voltage supplying circuit adjusts the common electrode voltages so that luminance and color variation of the pixels are corrected so that a visual angle with respect to a liquid crystal panel, seen from an arbitrary position in an up-and-down direction, is wider than a visual angle in a case where the common electrode voltages of all the groups are equal to each other [0006-0018].

24. In regards to claim 20, Nakao teaches wherein the common voltage supplying circuit includes: an input terminal for receiving a voltage which functions as a standard voltage of the common electrode voltages; a resistance element whose one end is connected to the input terminal; a constant current source for causing a constant current to flow to the resistance element; an output terminal [0067-0072], connected to other end of the resistance element, which outputs an output voltage; and a data latch circuit for outputting adjustment data, in accordance with which (i) a current value of the constant current caused to flow by the constant current source and (ii) a direction in which the constant current caused to flow are switched, to the constant current source (fig. 2 (42)).

25. In regards to claim 21, Nakao teaches comprising: a scanning line driving circuit for driving the scanning lines; and a reference voltage generating circuit for generating reference voltages, having plural levels different from each other, which are supplied to the scanning line driving circuit so as to make gradation display in accordance with a display signal, said reference voltage generating circuit being capable of adjusting the reference voltages (fig. 6 D, S1 and Power supply).

26. In regards to claim 22, Nakao teaches wherein the reference voltage generating circuit adjusts the reference voltages so that a predetermined gamma characteristic is

obtained in an arbitrary line of lines each of which is constituted of the pixels provided in a direction in which the scanning lines are disposed (fig. 5 and [0089]).

27. In regards to claim 23, Nakao teaches comprising a correction information storage circuit for storing adjustment amounts of the reference voltages, wherein the reference voltage generating circuit adjusts the reference voltages in accordance with the adjustment amounts stored in the correction information storage circuit (fig. 1 (43)).

28. In regards to claim 24, Nakao teaches wherein the reference voltage generating circuit adjusts the reference voltages so that a gamma characteristic is obtained in a line, constituted of the pixels, which is positioned on the one side in a direction in which the scanning lines are disposed and another gamma characteristic is obtained in a line, constituted of the pixels, which is positioned on the other side in the direction in which the scanning lines are disposed, said gamma characteristics being different from each other (fig. 5 [0089]).

29. In regards to claim 25, Nakao teaches wherein the reference voltage generating circuit adjusts the reference voltages so as to obtain gamma characteristics different from each other in a first line constituted of the pixels provided on the one side in a direction in which the scanning lines are disposed, a second line constituted of the

pixels provided on the other side in the direction in which the scanning lines are disposed, and a third line constituted of the pixels provided between the first line and the second line so that the gamma characteristic obtained in the third line is intermediate between the gamma characteristic obtained in the first line and the gamma characteristic obtained in the second line (fig. 5 [0089]).

30. In regards to claim 26, Nakao teaches wherein: the reference voltage generating circuit adjusts the reference voltages so as to obtain a gamma characteristic which causes luminance to decrease in a numerical order of the scanning lines in a case of using a liquid crystal panel whose luminance increases while a view point is moving from an upper direction to a lower direction with respect to the liquid crystal panel when an observer faces the liquid crystal panel, and the reference voltage generating circuit adjusts the reference voltages so as to obtain a gamma characteristic which causes the luminance to increase in a numerical order of the scanning lines in a case of a liquid crystal panel whose luminance decreases while the view point is moving from the upper direction to the lower direction with respect to the liquid crystal panel when the observer faces the liquid crystal panel (fig. 5, [0089, and 0018-0049]).

31. In regards to claim 27, Nakao teaches wherein: the common electrode voltage supplying circuit adjusts the common electrode voltages so that the luminance decreases in the numerical order of the scanning lines in the case of using the liquid

crystal panel whose luminance increases while the view point is moving from the upper direction to the lower direction with respect to the liquid crystal panel when the observer faces the liquid crystal panel, and the common electrode voltage supplying circuit adjusts the common electrode voltages so that the luminance increases in the numerical order of the scanning lines in the case of using the liquid crystal panel whose luminance decreases while the view point is moving from the upper direction to the lower direction with respect to the liquid crystal panel when the observer faces the liquid crystal panel (fig. 5, [0089, and 0018-0049]).

32. In regards to claim 29, Nakao teaches wherein the common electrodes of the pixels are divided into a plurality of groups, and the common electrode voltages are respectively adjusted so as to be adjusted independently every groups (fig. 11 V64-V0 and [0015]. "This gray scale display reference voltage generating circuit 39 is constructed of nine gray scale voltage input terminals indicated by V0, V8, V16, V24, V32, V40, V48, V56 and V64, resistor elements R0 through R7 having a resistance ratio for gamma correction and a total of 64 resistors (not shown) that are in groups of eight serially connected across both terminals of the resistor elements R0 through R7.") .

33. In regards to claim 30, Nakao teaches comprising the step of generating reference voltages, having plural levels, which cause gradation display to be made in accordance with a display signal, and adjusting the reference voltages ("There is

provided a gray scale display reference voltage generating circuit that can change a gamma correction characteristic in accordance with a liquid crystal material and LCD panel characteristics. Resistor elements R0 through R7 have a resistance ratio for gamma correction and generate gamma-corrected intermediate voltages on the basis of voltages across both input terminals V0 and V64. A gamma correction adjustment circuit 42 adjusts the gamma-corrected intermediate voltages upward or downward on the basis of adjustment data." abstract).

34. In regards to claim 31, Nakao teaches wherein the reference voltages are adjusted so that a predetermined gamma characteristic is obtained in an arbitrary line of lines each of which is constituted of the pixels provided in a direction in which the scanning lines are disposed (fig. 5, [0089 and 0018-0049]).

35. In regards to claim 32, Nakao teaches wherein the common electrode voltages are adjusted so that luminance and color variation of the pixels are corrected so that a visual angle with respect to a liquid crystal panel, viewed from an arbitrary position, is wider than a visual angle in a case where the common electrode voltages of all the groups are equal to each other (fig. 5, [0089, and 0018-0049]).

36. In regards to claim 33, Nakao teaches wherein the common electrode voltages are adjusted so that luminance and color variation of the pixels are corrected so that a visual angle with respect to a liquid crystal panel, viewed from an arbitrary position in an up-and-down direction, is wider than a visual angle in a case where the common electrode voltages of all the groups are equal to each other (fig. 5, [0089, and 0018-0049]).

37. In regards to claim 34, Nakao teaches wherein the common electrodes in each of the pixels are sequentially grouped for n lines of the scanning lines (n includes one), where n is a positive integer (fig. 6 scanning lines and fig. 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta
December 29, 2007

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